IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	10/621,067	§ Confirmation No.:	1252
Applicant:	Keith Farkas	§	
Filed:	07/16/2003	§	
TC/A.U.:	2195	§	
Examiner:	Kenneth Tang	§	
Title:	HETEROGENEOUS PROCESSOR CORE SYSTEMS FOR IMPROVED THROUGHPUT	§	
Docket No.:	200210109-1 (HPC.0762US)	§	

DECLARATION UNDER 37 C.F.R. § 1.132

We, Keith Farkas, Norman Paul Jouppi and Parthasarathy Ranganathan, state as follows:

1. We are the inventors of the subject matter of the present application (referenced above);

2. Rakesh Kumar and Dean M. Tullsen are not co-inventors of the present application.

3. At the time of the present invention, Keith Farkas was employed at Hewlett Packard. Norman Paul Jouppi is the Director of the Exascale Computing Lab at Hewlett Packard Labs. Parthasarathy Ranganathan is a Distinguished Technologist at Hewlett Packard Labs.

4. We conceived of the invention claimed in the present application and had a number of discussions regarding the subject heterogeneous multi-core processor technology before contacting Dean M. Tullsen and Rakesh Kumar.

5. While the invention had already been fully conceived and discussed, it was evident that simulations were appropriate to determine the degree of performance improvement to be achieved by the heterogeneous multi-core processor technology.

6. After we had conceived of the invention, we called Dean M. Tullsen and Rakesh Kumar on a confidential basis to discuss performing possible simulations of the invention.

7. Dean M. Tullsen is a professor at the University of California at San Diego, and at that time was an advisor to Rakesh Kumar, who was one of his doctoral students.

8. Rakesh Kumar, as primary researcher, performed the simulation of the heterogeneous multi-core processor technology revealed to Rakesh Kumar and Dean M. Tullsen by us.

9. After the simulations showed that a significant performance improvement could be achieved by the invention, Rakesh Kumar, Dean M. Tullsen, Keith Farkas, Norman Paul Jouppi, and Parthasarathy Ranganathan began work on a paper titled "Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures" for the IEEE Computer Architecture Letters ("Multi-Core Architecture Paper"), attached as Exhibit A. The Multi-Core Architecture Paper was submitted in March 2003, and the final draft was submitted in April 2003.

10. As a result of the work performed during the simulations, various results were obtained, at least some of which were published in the Multi-Core Architecture Paper.

11. The content of the Multi-Core Architecture Paper relating to a heterogeneous multi-core processor that has multiple heterogeneous cores originated with or was obtained from Keith Farkas, Norman Paul Jouppi, and Parthasarathy Ranganathan, inventors of the present application.

12. We also state that the authors of the Multi-Core Architecture Paper derived their knowledge of the subject matter described in the Multi-Core Architecture Paper relating to heterogeneous multi-core processors that have multiple heterogeneous cores from the inventors (including inventors Keith Farkas, Norman Paul Jouppi, and Parthasarathy Ranganathan) of the present application.

13. We also state that the Multi-Core Architecture Paper describes the work of the inventors (including inventors Keith Farkas, Norman Paul Jouppi, and Parthasarathy Ranganathan) of the present application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

9/29/2009
DATE

KEITH FARKAS

DATE

NORMAN PAUL JOUPPI

DATE

PARTHASARATHY RANGANATHAN

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

DATE

KEITH FARKAS

9/29/2009
DATE

NORMAN PAUL JOUPPI

9/29/2009
DATE

PARTHASARATHY RANGANATHAN